Refine Search

Search Results -

Term	Documents
(2 AND 8).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	0
(L2 AND L8).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L26

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, November 08, 2006 **Purge Queries** Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L26	l2 and l8	0	L26
L25	l2 and l7	0	L25
L24	l2 and l6	2	L24
L23	l2 and l5	4	L23
L22	l4 and l8	8	L22
L21	l4 and l7	2	L21
L20	l4 and l6	3	L20
L19	l4 and l5	3	L19
L18	l1 and l8	1	L18
L17	l1 and l7	3	L17
L16	l1 and l6	2	L16

L15	l1 and l5	4	L15
L14	l10 and l8	22	L14
L13	l10 and l7	45	L13
L12	l10 and l6	3	L12
L11	l10 and l5	25	L11
L10	boolean and short$4 near4 circuit$3 and (conjugat$4 or "OR" or "AND")	1042	L10
DB=PGPB,USPT; PLUR=YES; OP=OR			
L9	boolean and short$4 near4 circuit$3 and (conjugat$4 or "OR" or "AND")	1023	L9
L8	(326/41,114,125)[CCLS]	1674	L8
L7	(716/16-19)[CCLS]	3368	L7
L6	(712/200-203,223, 225,227,228)[CCLS]	1014	L6
L5	(712/2-300)[CCLS]	12758	L5
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	(programmable or programable or interact$5 or dynamic$6) near25 boolean and short$4 near4 circuit$3	73	L4
L3	dynamic$6 near25 boolean and short$4 near4 circuit$3	13	L3
L2	l1 and static$4	18	L2
L1	boolean and short$4 near4 circuit$3 near15 (conjugat$4 or "OR" or "AND")	50	L1

END OF SEARCH HISTORY

Results for "((boolean <and> short" <near/4> circuit")<in>metadata)"

e-mail

Your search matched **13** of **1430374** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

1. **Undetectability of Bridging Faults and Validity of Stuck-At Fault Test Sets**
   Kodandapani, K.L.; Pradhan, D.K.;
   Computers, IEEE Transactions on
   Volume C-29, Issue 1, Jan 1980 Page(s):55 - 59
   AbstractPlus | Full Text: PDF(1016 KB) IEEE JNL
   Rights and Permissions

2. **On the Impossible Class of Faulty Functions in Logic Networks Under Short Circuit Faults**
   Bhattacharya, B.B.; Gupta, B.;
   Computers, IEEE Transactions on
   Volume C-35, Issue 1, Jan 1986 Page(s):85 - 90
   AbstractPlus | Full Text: PDF(1376 KB) IEEE JNL
   Rights and Permissions

3. **Detection of stuck-at and bridging faults in Reed-Muller canonical (RMC) networks**
   Damaria, T.; Karpovsky, M.;
   Computers and Digital Techniques, IEE Proceedings-
   Volume 136, Issue 5, Sep 1989 Page(s):430 - 433
   AbstractPlus | Full Text: PDF(312 KB) IEE JNL

4. **Electrical behavior of GOS fault affected domino logic cell**
   Comte, M.; Ohtake, S.; Fujiwara, H.; Renovell, M.;
   Electronic Design, Test and Applications, 2006. DELTA 2006. Third IEEE International Workshop c
   17-19 Jan. 2006 Page(s):7 pp.
   Digital Object Identifier 10.1109/DELTA.2006.42
   AbstractPlus | Full Text: PDF(536 KB) IEEE CNF
   Rights and Permissions

5. **Testing for resistive shorts in FPGA interconnects**
   Haixia Gao; Yintang Yang; Xiaohua Ma; Gang Dong;
   Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on
   21-23 March 2005 Page(s):159 - 163
   Digital Object Identifier 10.1109/ISQED.2005.120
   AbstractPlus | Full Text: PDF(152 KB) IEEE CNF
   Rights and Permissions

6. **Delay testing of MOS transistor with gate oxide short**

Renovell, M.; Galliere, J.M.; Azais, F.; Bertrand, Y.;
Test Symposium, 2003. ATS 2003. 12th Asian
16-19 Nov. 2003 Page(s):168 - 173
Digital Object Identifier 10.1109/ATS.2003.1250804

AbstractPlus | Full Text: PDF(297 KB) IEEE CNF
Rights and Permissions

7. **Test escapes: analysis of short defect**
Renovell, M.; Azdis, F.; Bertrand, Y.;
Integrated Circuits and Systems Design, 1999. Proceedings. XII Symposium on
29 Sept.-2 Oct. 1999 Page(s):160 - 163
Digital Object Identifier 10.1109/SBCCI.1999.803111

AbstractPlus | Full Text: PDF(40 KB) IEEE CNF
Rights and Permissions

8. **Automatic test pattern generation for Iddq faults based upon symbolic simulation**
Ribas-Xirgo, L.; Carrabina-Bordoll, J.;
IDDQ Testing, 1996., IEEE International Workshop on
24-25 Oct. 1996 Page(s):94 - 98
Digital Object Identifier 10.1109/IDDQ.1996.557840

AbstractPlus | Full Text: PDF(412 KB) IEEE CNF
Rights and Permissions

9. **A fault model and a test method for analog fuzzy logic circuits**
Weiner, S.;
Test Conference, 1995. Proceedings., International
21-25 Oct. 1995 Page(s):282 - 291
Digital Object Identifier 10.1109/TEST.1995.529843

AbstractPlus | Full Text: PDF(876 KB) IEEE CNF
Rights and Permissions

10. **Accurate logic-level power estimation**
Bogliolo, A.; Ricco, B.; Benini, L.; De Micheli, G.;
Low Power Electronics, 1995., IEEE Symposium on
9-11 Oct. 1995 Page(s):40 - 41
Digital Object Identifier 10.1109/LPE.1995.482455

AbstractPlus | Full Text: PDF(212 KB) IEEE CNF
Rights and Permissions

11. **Faster circuits and shorter formulae for multiple addition, multiplication and symmetric Boo**
Paterson, M.S.; Pippenger, N.; Zwick, U.;
Foundations of Computer Science, 1990. Proceedings., 31st Annual Symposium on
22-24 Oct. 1990 Page(s):642 - 650 vol.2
Digital Object Identifier 10.1109/FSCS.1990.89586

AbstractPlus | Full Text: PDF(644 KB) IEEE CNF
Rights and Permissions

12. **Valid clocking in wavepipelined circuits**
Lam, W.K.C.; Brayton, R.K.; Sagiovanni-Vincentelli, A.;
Computer-Aided Design, 1992. ICCAD-92. Digest of Technical Papers., 1992 IEEE/ACM Internatio
8-12 Nov. 1992 Page(s):518 - 525
Digital Object Identifier 10.1109/ICCAD.1992.279318

AbstractPlus | Full Text: PDF(532 KB) IEEE CNF
Rights and Permissions

13. **On the design of reliable Boolean circuits that contain partially unreliable gates**
Kleitman, D.; Leighton, T.; Ma, Y.;
Foundations of Computer Science, 1994 Proceedings., 35th Annual Symposium on
20-22 Nov. 1994 Page(s):332 - 346

Digital Object Identifier 10.1109/SFCS.1994.365682